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Parallel and Distributed Systems, IEEE Transactions on
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3. **A performance comparison of the IBM RS/6000 and the Astronautics ZS-1**
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5. **Effective Instruction Prefetching in Chip Multiprocessors for Modern Commercia**
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High-Performance Computer Architecture, 2005. HPCA-11. 11th International Symposi
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6. **The effects of memory latency and fine-grain parallelism on Astronautics ZS-1 pe**
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8. **KSR1 multiprocessor: analysis of latency hiding techniques in a sparse solver**
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13-16 April 1993 Page(s):454 - 461

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Singh, G.B.; Abraham, S.G.; Westervelt, F.H.;
Circuits and Systems, 1993., Proceedings of the 36th Midwest Symposium on
16-18 Aug. 1993 Page(s):165 - 168 vol.1

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11. **Minimum register requirements for a module schedule**
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Microarchitecture, 1994. MICRO-27. Proceedings of the 27th Annual International Sym
30 Nov.-2 Dec. 1994 Page(s):75 - 84

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12. **Fast efficient simulation of write-buffer configurations**
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Eichenberger, A.E.; Abraham, S.G.;
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15. **Partitioning regular grid applications with irregular boundaries for cache-coherer multiprocessors**
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US-PAT-NO: 6772106

DOCUMENT-IDENTIFIER: US 6772106 B1

TITLE: Retargetable computer design system

---------- KWIC ---------

Brief Summary Text - BSTX (4):
A vast number of devices and appliances ranging from mobile phones, printers, and cars have **embedded computer systems**. The number of **embedded computer systems** in these devices far exceeds the number of general purpose computer systems such as personal computers or servers. In the future, the sheer number of these **embedded computer systems** will greatly exceed the number of general purpose computer systems.

Brief Summary Text - BSTX (5):
The design process for **embedded computer systems** is different from that for general purpose computer systems. There is greater freedom in designing **embedded computer systems** because there is often little need to adhere to standards in order to run a large body of existing software. Since **embedded computer systems** are used in very specific settings, they may be tuned to a much greater degree for specific applications. On the other hand, although there is greater freedom to customize and the benefits of customization are large, the revenue stream from a particular **embedded computer system** design is typically not sufficient to support a custom design.

Brief Summary Text - BSTX (6):
In the past, there have been a number of attempts at automating the design of **embedded computer systems**. In one, a template-based processor design space was automatically searched to identify a set of best solutions. In another, a framework for the design of retargetable, application-specific, very long instruction word (VLIW) processors was developed. This framework provided the tools to trade off architecture organization and compiler complexity. A hierarchical approach was proposed for the design of systems consisting of processor cores and instruction/data caches where a minimal area system that satisfied the performance characteristics of a set of applications was synthesized.

Brief Summary Text - BSTX (9):
In designing **embedded computer systems**, the general design space consists of a processor and associated Level-1 instruction, Level-1 data, Level-2 unified caches, and main memory. The number and type of functional units in the processor may be varied to suit the application. The size of each of the register files may also be varied. Other aspects of the processor such as whether it supports speculation or predication may also be changed. For each of the caches, the cache size, the associativity, the line size, and the number of ports can be varied. Given a subset of this design space for an application and its associated data sets, a design objective is to determine a set of cost-performance optimal processors and systems. A given design is cost-performance optimal if there is no other design with higher performance and lower cost.

Detailed Description Text - DETX (9):
Each computer design 47 is plotted on a cost/performance graph 46 as shown in FIG. 2. The set of points that are minimum cost at a particular performance level identify the set of best designs 48 or the **Pareto** curve. After the process is completed for one design, the spacewalker module 41 creates a new design and everything is repeated. The spacewalker module 41 uses cost and performance statistics of the previous design as well as characteristics of the application 42 to identify a new design that is likely to be profitable. The process terminates when there are no more likely profitable designs to investigate.